JEDEC STANDARD

Standard Description of 1.5 V CMOS Logic Devices

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STANDARD DESCRIPTION OF 1.5 V CMOS LOGIC DEVICES

(From JEDEC Board Ballot JCB-01-34, formulated under the cognizance of the JC-40.1 Subcommittee on CMOS/BiCMOS Digital Logic.)

1 Scope

This standard defines dc interface parameters and test loading for a CMOS digital-logic family based on 1.5 V (nominal) power supply levels and 1.5 V input tolerance.

The purpose is to provide a standard for 1.5 V nominal supply voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

2 Definitions for the purpose of this document

Prefixes:

Prefixes ”54” or ”74” immediately preceding family name indicate the operating temperature range. For example, 54XXX refers to the Military (MIL) version of devices which are specified over the temperature range of -55 °C to 125 °C. 74XXX refers to the Commercial (COM’L) version of devices that are specified over -40 °C to 85 °C.

3 Standard specifications

3.1 Absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1):

Supply voltage range, V_{DD} . . . . . –0.5 V to 2.0 V

Input voltage range, V_I: Except I/O ports . . . . . –0.5 V to V_{DD} + 0.5 V
I/O ports (see Note 1, 2) . . . . . –0.5 V to V_{DD} + 0.5 V

Output voltage range, V_O (see Note 1 and 2) . . . . . –0.5 V to V_{DD} + 0.5 V

Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) . . . . . - 50 mA

Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . . . . ± 50 mA

Voltage range applied to any output in the high-impedance state
or power - off state, V_O (see Note 1 and 2) . . . . . –0.5 V to V_{DD} + 0.5 V

Storage temperature range, Tstg . . . . . .–65 °C to 150 °C

NOTE 1 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 This value is limited to 2 V maximum.

3 Standard specifications (cont'd)

3.2 Recommended operating conditions (see Note 3):

		MIN	MAX	UNIT
V_{DD} Supply voltage	Operating	1.4	1.6	V
	Data Retention Only (optional spec.)	1		
V_{IH} High-level input voltage	V_{DD} = 1.4 V to 1.6 V	0.65 × V_{DD}	V_{DD} + 0.3	V
V_{IL} Low-level input voltage	V_{DD} = 1.4 V to 1.6 V	–0.3	0.35 × V_{DD}	V
V_I Input voltage		0	V_{DD}	V
V_O Output voltage		0	V_{DD}	V
?t/?v Input transition rise or fall rate (see Note 4)		0	10	ns/V
T_A Operating free-air temperature	54 Series	–55	125	°C
	74 Series	–40	85	

NOTE 3 All unused inputs of the device must be held at V_{DD} or GND to ensure proper device operation.

NOTE 4 As measured between V_{IL}(max) and V_{IH}(min).

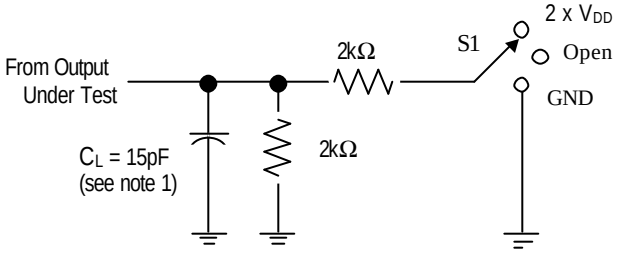
3.3 Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 5):

PARAMETER	TEST CONDITIONS	V_{DD}	MIN	MAX	UNIT
V_{OH}	I_{OH} = –100 µA	1.4 V	1.2 V		V
	I_{OH} = –2 mA V_{IH} = 0.91 V, V_{IL} = 0.49 V	1.4 V	0.75 × V_{DD}		
V_{OL}	I_{OL} = 100 µA	1.4 V		0.2	V
	I_{OL} = 2 mA V_{IH} = 0.91 V, V_{IL} = 0.49 V	1.4 V		0.25 × V_{DD}	
I_I	V_I = V_{DD} to GND	1.6 V		± 10	µA
I_{OZ} (see Note 6)	V_O = V_{DD} to GND	1.6 V		± 10	µA
I_{DD}	V_I = V_{DD} or GND I_O = 0	1.6 V		20	µA

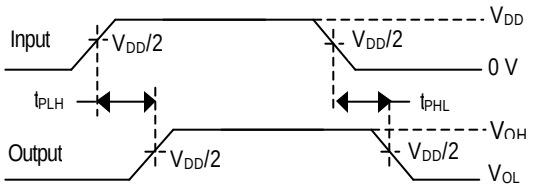
NOTE 5 V_{DD} of the sending and receiving devices must track within 0.1 V to maintain adequate dc margins.

NOTE 6 For I/O ports, the parameter I_{OZ} includes the input leakage current.

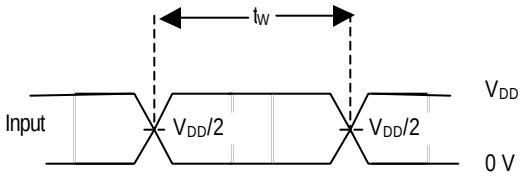
4 Test circuit and switching waveforms



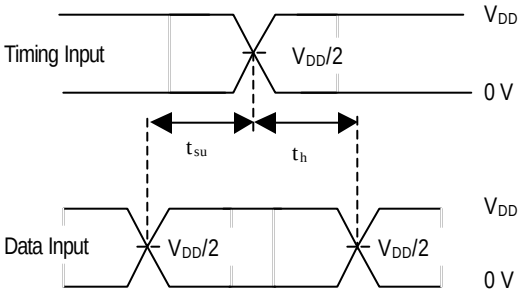
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 X V_{DD}
t_{PHZ}/t_{PZH}	GND



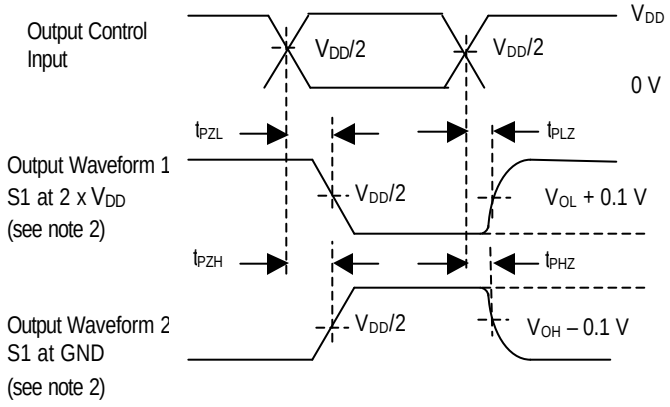
MEASUREMENT 1. PROPAGATION DELAY TIMES



MEASUREMENT 3. PULSE DURATION (WIDTH) MEASUREMENTS



MEASUREMENT 4. SETUP AND HOLD TIMES



MEASUREMENT 2. ENABLE AND DISABLE TIMES

NOTE 1 C_L includes probe, and jig capacitance.

NOTE 2 Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

NOTE 3 All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz, Z_O = 50 Ω, $t_r = t_f$ = 2 ns.

NOTE 4 The outputs are measured one at a time with one transition per measurement.

NOTE 5 t_{PLZ} and t_{PHZ} are the same as t_{dis}.

NOTE 6 t_{PZL} and t_{PZH} are the same as t_{en}.

NOTE 7 t_{PLH} and t_{PHL} are the same as t_{pd}.

6 Reference to other applicable JEDEC standards and publications

JESD8-11, *1.5 V± 0.1 V Power Supply Voltage and Interface Standard for Non-terminated Digital Intergrated Circuits,* October 2000.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